Agenda

- Q35 chipset - Overview
- Q35 emulation
- Q35-only features
- Q35 limitations
- Q35 use cases
# Q35 chipset - Overview

- Data sheet

## Essentials

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Status</td>
<td>Launched</td>
</tr>
<tr>
<td>Launch Date</td>
<td>Q3’07</td>
</tr>
<tr>
<td>Supported FSBs</td>
<td>1333MHz / 1066MHz / 800MHz</td>
</tr>
<tr>
<td>FSB Parity</td>
<td>No</td>
</tr>
<tr>
<td>Embedded Options Available</td>
<td>Yes</td>
</tr>
<tr>
<td>TDP</td>
<td>15 W</td>
</tr>
<tr>
<td>Recommended Customer Price</td>
<td>N/A</td>
</tr>
<tr>
<td>Datasheet</td>
<td>Link</td>
</tr>
</tbody>
</table>

## Memory Specifications

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Memory Size (dependent on memory type)</td>
<td>8 GB</td>
</tr>
<tr>
<td>Memory Types</td>
<td>DDR2 667/800</td>
</tr>
<tr>
<td>Max # of Memory Channels</td>
<td>2</td>
</tr>
<tr>
<td>Max Memory Bandwidth</td>
<td>6.4 GB/s</td>
</tr>
<tr>
<td>Physical Address Extensions</td>
<td>36-bit</td>
</tr>
</tbody>
</table>

## Expansion Options

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI Express Revision</td>
<td>1.1</td>
</tr>
<tr>
<td>PCI Express Configurations</td>
<td>1x16</td>
</tr>
</tbody>
</table>

## Advanced Technologies

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel® Virtualization Technology for Directed I/O (VT-d)</td>
<td>Yes</td>
</tr>
<tr>
<td>Intel® Fast Memory Access</td>
<td>No</td>
</tr>
<tr>
<td>Intel® Flex Memory Access</td>
<td>Yes</td>
</tr>
</tbody>
</table>

## Package Specifications

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Max CPU Configuration</td>
<td>1</td>
</tr>
<tr>
<td>T&lt;sub&gt;CASE&lt;/sub&gt;</td>
<td>105°C</td>
</tr>
<tr>
<td>Package Size</td>
<td>34 mm x 34 mm</td>
</tr>
<tr>
<td>Low Halogen Options Available</td>
<td>See MDDS</td>
</tr>
</tbody>
</table>
Q35 chipset - Overview

- Topology
  - North Bridge: MCH
  - South Bridge: ICH9

![Q35 Express Chipset Block Diagram](image-url)
Agenda

- Q35 chipset - Overview
- Q35 emulation
- Q35-only features
- Q35 limitations
- Q35 use cases
Q35 emulation

- Info qtree
Q35 emulation

- lspci

```
Q35
-------|
00:00.0 Host bridge: Intel Corporation 82G33/G31/P35/P31 Express DRAM Controller
00:01.0 VGA compatible controller: Device 1234:1111 (rev 02)
00:02.0 Ethernet controller: Intel Corporation 82540EM Gigabit Ethernet Controller (rev 03)
00:1f.0 ISA bridge: Intel Corporation 82801IB (ICH9) LPC Interface Controller (rev 02)
00:1f.2 SATA controller: Intel Corporation 82801IR/IO/IH (ICH9R/DO/DH) 6 port SATA Controller [AHCI mode]
00:1f.3 SMBus: Intel Corporation 82801I (ICH9 Family) SMBus Controller (rev 02)

I440FX
-------|
00:00.0 Host bridge: Intel Corporation 440FX - 82441FX PMC [Natoma] (rev 02)
00:01.0 ISA bridge: Intel Corporation 82371SB PIIX3 ISA [Natoma/Triton II]
00:01.1 IDE interface: Intel Corporation 82371SB PIIX3 IDE [Natoma/Triton II]
00:01.3 Bridge: Intel Corporation 82371AB/EB/MB PIIX4 ACPI (rev 03)
00:02.0 VGA compatible controller: Device 1234:1111 (rev 02)
00:03.0 Ethernet controller: Intel Corporation 82540EM Gigabit Ethernet Controller (rev 03)
```
Q35 emulation

- PCIe/PCI Topology
Q35 emulation

- PCI/PCIe devices placement
Q35 emulation

- PCIe/PCI ACPI Hotplug

Bus 0

Integrated PCIe Dev 1
Root Port 1
PCIe Dev 2

Bus 1

Switch

Upstream Port 1
Bus 3
Downstream Port 1
Bus 4

PCIe Dev 3

PCIe native hotplug

Bus 2

Root Port 2

Bus 5

Integrated PCIe Dev 1

DMI-PCI bridge

Bus 6

P2P bridge

PCI Dev 3

PCI ACPI hotplug

PCI Dev 2
Q35 emulation

- Virtio

PCIe + Pure virtio 1.0
(disable-legacy=on, disable-modern=off)

PCI + Transitional virtio
(disable-legacy=off, disable-modern=off)
Agenda

- Q35 chipset - Overview
- Q35 emulation
- Q35-only features
- Q35 limitations
- Q35 downstream
Q35-only features

- **PCIe “goodies”**
  - Extended configuration space (MMCFG)
  - PCIe native hotplug
  - Advanced Error Reporting (AER)
  - Alternative Routing-ID Interpretation (ARI)
  - Native Power Management
  - Function Level Reset (FLR)
  - Address Translation Services (ATS)

- **AHCI** storage controller

- **vIOMMU** emulation

- “Secure” **Secure Boot**
Agenda

- Q35 chipset - Overview
- Q35 emulation
- Q35-only features
- Q35 limitations
- Q35 downstream
Q35 limitations

- **No support** for legacy guests (Windows XP/2000).
- **Questionable support** for legacy QEMU devices.
- **Limited IO space** can affect the number of devices used by a single Q35 machine:
  - Each device behind a separate PCI bridge.
  - Each bridge requires 4K IO range.
  - Several solutions available:
    - Plug only PCIe devices into PCIe ports.
    - Use smaller/non-standard IO windows for bridges.
    - ...
Agenda

- Q35 chipset - Overview
- Q35 emulation
- Q35-only features
- Q35 limitations
- Q35 use cases
Q35 use cases

- Current use-cases:
  - **P2V** (migrate physical machine to VM)
  - **Secure boot** (+OVMF)
  - **vIOMMU** (NFV)
Thank you!